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Switched Boost Inverter With PWM Control And Development Of A Prototype Model

Shilpa A. S¹., H. Vasantha Kumar Shetty²

PG student (Power Electronics), Dept. of EEE, Dayananda Sagar College of Eng., Bangalore, India¹

Professor, Dept. of EEE, Dayananda Sagar College of Eng., Bangalore, India²

ABSTRACT: The objective in this paper is to study the operating modes and analysis of the Switched Boost Inverter (SBI). The performance of the proposed SBI is similar to that of Z-Source Inverter (ZSI). In comparison to the ZSI, the present topology results in lower volume and lower cost since it reduces the number of passive component. This feature makes it more suitable for low power applications than ZSI.

For the proper operation of the inverter, with special consideration to its operating principle (shoot-through i.e., conduction of two switches on the same leg of the inverter), a modified PWM control strategy is also described in detail. In addition, mathematical relations between various performance parameters under this modified PWM technique have been described in detail.

Simulation is carried out using Matlab/Simulink software to verify the theoretical analysis made. This report also presents a laboratory prototype of the Switched boost inverter along with it results.

KEYWORDS: Z-Source Inverter, Switched Boost Inverter, Modified PWM technique, Shoot-through, Non-Shoot-through.

I.INTRODUCTION

ZSI employs a unique impedance network to couple the converter circuit to the power source, thus providing unique characteristic features that cannot be found in the traditional Voltage source inverter and Current source inverter. The unique impedance network mentioned above, implements two capacitors and two inductors. Introduction of these passive components add weight and size to the whole inverter. In order to reduce size and weight, a new topology is considered which involves lesser passive components, meanwhile trying to attempt similarity in all the steady state performance. This new topology is called Switched Boost inverter, which is being studied and analysed in this report.

II. LITERATURE SURVEY

The basic idea of SBI [2] is derived from ZSI [1]. By controlling the shoot-through duty cycle, the ZSI can be able to produce any AC output voltage from a given DC input voltage. This feature makes the ZSI suitable for number of applications such as renewable power systems (photovoltaic and fuel cells), adjustable speed drives, general purpose motor drives, electric vehicles, uninterruptible power supplies [3]-[8] etc.

Conventional pulse-width modulation techniques can be modified strategically to affect the operation of ZSI continuously or discontinuously, while retaining all the harmonic performance features of the conventional modulation techniques [9]. The complete analytical performance of the ZSI using X-shaped LC impedance network is complicated. Hence a small signal model method is resorted in [10] to derive transfer function and asses the performance there upon. From literature survey it is evident that ZSI is a promising technology for both buck and boost operations. But ZSI has the drawback of employing more and bulky passive components. Therefore SBI topology has been proposed [2] to reduce the number of passive components, thus can be used in low power applications where size and weight matters.

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II.SWITCHED BOOST INVERTER

Fig. 1 shows the schematic arrangement of the SBI, which is a buck-boost type of DC-AC converter just like the classical ZSI. The major components like active switch(S), two diodes (D_a, D_b) , one inductor (L), and one capacitor (C) are interposed between voltage source, V_g and the inverter bridge. These components form the switched boost network of the SBI. A low pass filter is used at the output of the inverter bridge to filter the switching frequency components in the output voltage of H-bridge, V_{AB} . L_f and C_f form the filter circuit. R_L is the load. V_o is the final output of the inverter bridge after filtering the switching frequency components in V_{AB} .

The circuit of SBI makes use of the MOSFET switches S, S1, S2, S3 and S4. However, one can also think of IGBT version with proper integration of the gate circuit. V_{sn1} denotes switch node-1 voltage and V_i denotes the switch node-2 voltage or inverter input voltage or DC link voltage. V_C is the capacitor voltage.

In order to analyse the steady state characteristics of SBI, consider T_s be one switching cycle time (time taken to finish one complete cycle) and the D be the duty cycle (amount of time the signal is in a high state as a percentage of the total time it takes to complete one cycle).



Fig. 1 Circuit diagram of the SBI

For the of steady-state analysis, the operating states are divided into shoot-through and non-shoot-through states. Initially, the inverter is assumed to be in shoot-through state for duration $D.T_S$ during switching cycle T_S . The switch S is turned on during this interval. The inverter bridge is shorted through upper and lower switching devices in the phase legs. The equivalent diagram is as shown in Fig. 2a. During the shoot-through state, the inverter bridge will be short circuited. Diodes Da and Db are reverse biased as $V_C > V_g$. Capacitor C charges the inductor L through switch S and the inverter bridge. The inductor current in this interval equals the capacitor discharging current.

For the remaining duration in the switching cycle i.e., $(1 - D).T_{S_{s}}$ the inverter will be in non-shoot-through state. The switch S is turned off. In this interval the inverter bridge is represented by a current source as shown in Fig. 2b. During the non-shoot-through, the V_g and L together supply power to the inverter and the capacitor through D_a and D_b. The inductor current in this interval equals to the sum of capacitor charging current and the inverter input current.



Fig. 2 Operating states of the SBI a) shoot-through state b) non-shoot through state.

Referring to the Fig. 2a and Fig. 2b we can write the following expressions.

$$v_{L}(t) = \begin{vmatrix} v_{C}(t), & \text{if } 0 < t < D.T_{S} \\ V_{S} - v_{C}(t), & \text{if } D.T_{S} < t < T_{S} \end{vmatrix}$$
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Vol. 3, Issue 8, August 2014

$$i_{C}(t) = \begin{vmatrix} -i_{L}(t), & \text{if } 0 < t < D.T_{S} \\ i_{L}(t) - i_{i}(t), & \text{if } D.T_{S} < t < T_{S} \end{vmatrix}$$
(2)

$$v_i(t) = \begin{vmatrix} 0, & if \ 0 < t < D.Ts \\ v_C(t) & if \ D.Ts < t < Ts \end{vmatrix}$$
(3)

From the linear ripple approximation, (1)-(3) can be written as

$$v_L(t) = \begin{vmatrix} V_C, & \text{if } 0 < t < D.T_S \\ V_S - V_C, & \text{if } D.T_S < t < T_S \end{vmatrix}$$

$$\tag{4}$$

$$ic(t) = \begin{vmatrix} -I_L, & \text{if } 0 < t < D.T_S \\ I_L - I_i, & \text{if } D.T_S < t < T_S \end{vmatrix}$$

$$(5)$$

$$vi(t) = \begin{vmatrix} 0, & if \ 0 < t < D.T_s \\ V_C, & if \ D.T_s < t < T_s \end{vmatrix}$$
(6)

In the above expressions V_C and I_L are DC components in $v_C(t)$ and $i_L(t)$ and I_i is the current drawn by the inverter bridge in the (1–D).T_S interval. Under steady-state condition, we can write

$$V_C.D + (V_S - V_C).(1 - D) = 0 \Longrightarrow \frac{V_C}{V_S} = \frac{1 - D}{1 - 2D}$$
(7)

$$-I_{L}.D + (I_{L} - I_{i}).(1 - D) = 0 = \frac{I_{L}}{I_{i}} = \frac{1 - D}{1 - 2D}$$
(8)

$$V_i = 0.D + V_C \cdot (1 - D) = V_C \cdot (1 - D)$$
⁽⁹⁾

From (7) it is clear that the conversion ratio (V_C/V_g) varies with the duty cycle. (V_C/V_g) is unity when D = 0, and it becomes very high as D approaches 0.5.

Note: The shoot-through duty ratio (D) of the SBI cannot exceed 0.5.

III. PWM CONTROL OF SWITCHED BOOST INVERTER

A modified PWM control strategy [2] is used for the proposed SBI based on the traditional sine-triangle PWM. In this scheme the switching losses have been reduced and here the switching frequency of S is always constant. $v_{tri}(t)$ is a high frequency triangular carrier of amplitude V_P and having frequency f_s . $v_m(t)$ and $-v_m(t)$ are the sinusoidal modulation signals of amplitude M.V_P (M is the modulation index) and having frequency f_o . The f_s is chosen such that, it is much greater than the f_o . Due to this reason, $v_m(t)$ is nearly constant during a switching cycle.

The signals ST₁ and ST₂ are generated by comparing $v_{tri}(t)$ with constant voltages, V_{ST} and $-V_{ST}$ respectively. The gate control signals for switch S₁(G_{S1}) and switch S₂(G_{S2}) are generated by comparing $v_m(t)$ and $-v_m(t)$ with $v_{tri}(t)$. The gate control signals for switch S₃ (G_{S3}) is generated by NAND operation on ST1 and G_{S2} and the gate control signals for switch S (G_{S3}) are generated by NAND operation on ST2 and G_{S1}. The gate control signals for the switch S (G_S) are generated by NAND operation on ST2 and G_{S1}. The gate control signals for the switch S (G_S) are generated by NAND operation on ST2 and G_{S1}.



(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 8, August 2014

The following relations have been established for the proper operation of the SBI using modified PWM technique. 1. Relation between constant voltage (VST) and shoot-through duty ratio

$$v_{tri}(t) = \begin{vmatrix} -V_p \\ T_s / 4 \\ (t - \frac{T_s}{4}), & if \ 0 < t < \frac{T_s}{2} \\ -V_p \\ T_s / 4 \\ (t - \frac{3T_s}{4}), & if \ \frac{T_s}{2} < t < T_s \end{vmatrix}$$
(10)
$$v_{tri}(t_1) = v_{tri}(t_2) = -V_{ST} \quad t_2 - t_1 = \frac{DT_s}{2}$$
(11)

Substituting (11) in (10), t_1 and t_2 can be given as

.

$$v_{tri}(t_{1}) = -V_{ST} = \frac{-V_{P}}{T_{S}/4} \left(t_{1} - \frac{T_{S}}{4} \right)$$

$$v_{tri}(t_{2}) = -V_{ST} = \frac{V_{P}}{T_{S}/4} \left(t_{2} - \frac{3T_{S}}{4} \right)$$

$$t_{1} = \frac{T_{S}}{4} \left(1 + \frac{V_{ST}}{V_{P}} \right) \quad t_{2} = \frac{T_{S}}{4} \left(3 - \frac{V_{ST}}{V_{P}} \right)$$
(12)

Substituting t_1 and t_2 in (11)

$$D = 1 - \frac{V_{ST}}{V_P}$$
(13)

2. Relation between shoot-through duty ratio and modulation index

To ensure that the shoot-through is not going to affect the power interval, D value should be selected such that the total width of the shoot-through interval should be less than the total available width of the interval with zero value in any switching cycle. This can be written as

$$D.T_{s} < T_{s} - \max\left(\frac{v_{m}(t).T_{s}}{V_{p}}\right)$$

$$D < 1 - M$$
(14)
(15)

Where, modulation index can be given as:

$$M = \max(v_m(t)/V_P)$$

3. Relation between constant voltage (VST) and modulation index From (13) and (15), it can be written as

$$1 - \frac{V_{ST}}{V_P} = 1 - M$$
$$V_{ST} > MV_P$$

(16)

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(An ISO 3297: 2007 Certified Organization)

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IV.RESULTS AND DISCUSSION

Simulation is carried out using Matlab/Simulink software. The simulink model is as shown in Fig. 3. Modified PWM technique has been used here. V_{ST} is a constant, whose value is 0.75. Multimeter is used to measure the voltage across the capacitor C. Refer Chapter 3 for the details of the modified PWM technique employed in SBI.

Calculations of various voltages in SBI are shown in Table 1. Two sets of calculations have been made, keeping the duty cycle same but with different input voltage and different modulation index. The first set is intended for the comparison of SBI with that of ZSI. Input voltage considered in the first set is high i,e 100 and M=0.48. The second set is used to verify the hardware results. Input voltage considered in second set is less i,e 17 V and M=0.63. The switching frequency is 10 kHz and D=0.3 in both the cases. In the simulation, all of the components are assumed ideal. L=5mH, C=100µF and R_L= 1k\Omega. The following waveforms are obtained:



Fig. 3 Simulink model of the SBI

Table 1 Calculation of various voltages in ZSI and SBI

Voltage	SBI			ZSI	
	Formula	Value	Value	Formula	Value
V_{g}	-	100 V	17 V	-	100 V
V _C	$\frac{V_g(1-D)}{1-2D}$	217 V	28 V	$\frac{V_g(1-D)}{1-2D}$	175
$\stackrel{\wedge}{V_i}$	V _C	217 V	28 V	$\frac{V_C}{1-D}$	250
$\stackrel{\wedge}{V_o}$	$\stackrel{\wedge}{V_i}.M$	140 V	19 V	$\stackrel{\wedge}{V_i}.M$	140



(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 8, August 2014



Fig. 4 shows the voltage across the capacitor in SBI. The capacitor voltage is boosted to nearly 1.7V times the input voltage in steady state i.e., 28V. In case of SBI, the capacitor voltage is equal to the inverter input voltage. So the input voltage to the inverter is also boosted nearly 1.7 times the input voltage.



Fig. 5 shows the output voltage of H-bridge in SBI. The V_{AB} is 29V. The output of the H-bridge is usually a square wave. To make this into sine wave output, a low-pass LC filter is used on the output side of the inverter.



Fig. 6 Output voltage of SBI for an input of 17V

Fig. 6 shows the inverter output voltage after filtering the switching frequency components in the output voltage of Hbridge. The output voltage is 19 V. The waveforms obtained through SBI simulation do confirm the mathematical analysis made in Table 1

V. EXPERIMENTAL VERIFICATION

The photograph of the SBI prototype is shown in Fig. 7. The prototype is explained by dividing the entire setup into three functional blocks. The first is the controller circuit, the second is the gate driver circuit and the third is the main SBI circuit.



(An ISO 3297: 2007 Certified Organization) Vol. 3, Issue 8, August 2014 Driver Circuit for Si, 52, 53, 54 Driver circuit for S High frequency controller circuit Low frequency controller circuit Low frequency controller circuit

Fig. 7 Photo of the laboratory prototype of SBI

The controller circuit gives the control signals which operate the gate driver circuit. The gate driver circuit will drive the respective switches of the SBI circuit. The working of each circuit is explained in detail as below:

1.Controller circuit: The AT89S52 is a low-power, high-performance CMOS 8-bit microcontroller. It is a very popular, low cost, general purpose microcontroller due to their industry standard instruction set. There are two controller circuits. One is used for high frequency i.e., for controlling the main switch, S. The other is used for low frequency control i.e., for controlling other switches S1, S2, S3 and S4.

230 V AC will be stepped down to 12V AC using step-down transformer. The 5V AC will be rectified and regulated by the rectifier and regulator provided on the controller circuit. The resulting 5V DC will be given as input to the controller IC. Controller IC i.e., AT89S52 will provide an output of 5 V pulse. The 5V pulse will be fed to the buffer IC of the gate driver circuit.

2.Gate driver circuit: 5V pulse from the controller IC will be strengthened using the buffer amplifier i.e., the current will be increased but the voltage remains the same. The output of the buffer amplifier is 5V dc. The output of the buffer IC will be given as the input to the opt coupler IC. An opto-isolated gate driver is used in order to provide isolation between the low power controller circuit and the main SBI circuit. Due to the opto-isolation, signals strength may deteriorate. To overcome this, TTL (Transistor Transistor Logic) and transformer combination is used. Generally speaking, TTL use NPN and PNP type bipolar junction transistors.

3. SBI circuit: 230V AC is stepped down to 12V AC using a step-down transformer. Output of the transformer is rectified using diode bridge rectifier and rectified DC voltage is fed as input to the SBI circuit. The SBI output voltage is measured across the load R_L . Outputs are obtained using the laboratory prototype of the SBI shown in Fig. 8. The result of the laboratory prototype is used to verify the theoretical analysis simulation results.



Fig. 8 Results of laboratory prototype of SBI a)Output of the high frequency controller circuit. B) Output of low frequency controller c) input to the optocoupler ic d) output of the optocoupler ic e) gate signals of switch S f) inverter output V_0 .

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(18)

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(An ISO 3297: 2007 Certified Organization)

Vol. 3, Issue 8, August 2014

Fig. 8a shows the output of the high frequency controller. The output is obtained at Pin. 1 of high frequency controller IC. As mentioned earlier the output of the controller IC is a 5V pulse. Its frequency is 10 kHz. Fig. 8b shows the output of the low frequency controller. The output is obtained at Pin. 1 of low frequency controller IC. In case of low frequency controller IC also the output is a 5V pulse. But as its name says the frequency is less. Its frequency is 50 Hz. Fig. 8c shows the input to the opt coupler IC. The input voltage here is very less i.e., 1.2 V. The optocoupler stage provides isolation between the low power controller circuit and the main SBI circuit. Due to the opto-isolation, signals strength may deteriorate. To overcome this, TTL and transformer combination is used. Fig. 8d shows the output of the optocoupler IC. Compared with the input stage the output signal strength has been increased it is due to the TTL logic implemented. Signal has a magnitude of around 15V here. This signal is used to the turn on the switches of SBI. Fig. 8e shows the gate control signals of switch S. The switching frequency here is high i.e., 10 kHz. It operates at a duty cycle 0.3 as shown. Whenever the gate signal to the S is high i.e., G_S is high, the V_i will be low and vice-versa. Fig. 8f shows the inverter output voltage. For a given input voltage of 17V, the output has been boosted to 18.5 V.

VI COMPARISON OF SBI AND ZSI

1. Comparison of the Boost Ability: The peak dc-link voltage across the inverter circuit, to the dc input is termed as the boost factor. The boost factor for the SBI (B_{SBI})and ZSI (B_{ZSI})can be given by

$$B_{SBI} = \frac{1 - D}{1 - 2D} \quad B_{ZSI} = \frac{1}{1 - 2D} \tag{17}$$

The boost ability of the SBI inverter is lesser than that of ZSI[1] and SBI. 2. Comparison in terms of Voltage conversion ratio versus Modulation index: The voltage conversion ratio for SBI (G_{SBI}) and ZSI (G_{ZSI}) can be given as:

$$G_{SBI} = \frac{M^2}{2M - 1}$$
 $G_{ZSI} = \frac{M}{2M - 1}$

Compared with the ZSI using the same modulation index, the SBI provides a higher voltage boost inversion. Therefore, for the same gain, the SBI use a higher modulation index in order to improve the inverter output quality.

2. Comparison of maximum voltage stress: Table 2 lists the maximum voltage stress across the switches for ZSI and SBI. It shows that the SBI provides a lower voltage stress across the active switches.

Table 2

Comparison of max	ximum stress ad	cross the	switches
No. of active	ZSI	SBI	
S1 to S4	$V_T = \stackrel{\wedge}{V_i}$	250	217
S	$V_{T1} = V_C - V_g$	-	117

4. Comparison of number of components: The SBI uses two passive components and three semiconductor switches, while ZSI uses four passive components and one semiconductor switch. Due to the less number of passive component, the SBI may lead to reduction in the size and weight of the overall power converter when compared to a ZSI. But increases in the number of semiconductor devices, the SBI requires a better protection circuit when compared to ZSI.

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